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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,545	02/27/2004	Javier Arguelles	1406/186	7090

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EXAMINER
HE, AMY

ART UNIT	PAPER NUMBER
2831	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/788,545	ARGUELLES ET AL.	
	Examiner	Art Unit	
	AMY HE	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *26 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-12* is/are allowed.

6)☒ Claim(s) *1-4,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-3, 13, 14 are rejected under 35 U.S.C. 103(a)'as being unpatentable over Oliva (US 2007/0188187) in view of Whetsel (US 6,731,106 B2).

The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1,148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Re claim 1, Oliva disclosed switching circuit for a high speed data interface of an integrated circuit comprising switching transistors (504,802)(Fig. 5,8) for switching termination resistor 506 (Fig. 5) output stage (programmable resistance element) of a data transmission signal path to a termination resistor 514 input stage (chip boundary) of a data reception signal path to form an internal feedback test loop (502, 506, pad, 508 forms the feedback loop shown in Fig. 5) within said integrated circuit.

Oliva did not expressly disclose switching transistors, which switch in a test mode.

Whetsel disclosed switching circuit for test mode operation for measuring on-resistance of an output stage (output buffer)(column 15 line 49).

At the time the invention was made it would have been obvious for one of ordinary skill in the art to modify Oliva et al. by including test mode operation disclosed by Whetsel in the impedance control circuit of Oliva for measuring on-resistance of output stage.

Re claims 2 and 3, Oliva disclosed switching circuit is connected to a configuration register 502 the termination resistor output stage 506 is programmable. The impedance element control circuit 502 is broadly interpreted as comprising configuration register since it produces one or more program control output signals to program or affect the programming of the programmable resistance element 506 (paragraph 0040).

Re claims 13 and 14, Oliva disclosed high speed data interface within an integrated circuit comprising:

(a) a transmitting signal path for transmitting data via a data transmission line (output path from 506 to pad) which is connected to a termination resistor output stage 506 of said data transmission signal path, wherein the termination resistor output stage 506 is provided for adapting the output impedance of said data transmission signal path to a load (see claim 2 line 4) connected to said transmission data line;

(b) a reception data signal path for receiving data via a data reception line (input line connected to pad), which is connected to a termination resistor 514 input stage of said data reception signal path, wherein the termination resistor 514 input stage is

provided for adapting the input impedance of said data reception signal path to a load (claim 2 line 4) connected to said reception data line; and

(c) a controllable switching circuit 502,504,506 comprising switching transistors for connecting termination resistor Output stage 506 to the termination resistor input stage 514 to form an internal feedback test loop within said integrated circuit (502, 506, pad, 508 forms the feedback loop shown in Fig. 5).

Oliva did not expressly disclose controllable test switching circuit switching in a test mode.

Whetsel disclosed Switching circuit for test mode operation for measuring on-resistance of an output stage (output buffer) (column 15 line 49).

At the time the invention was made it would have been obvious for one of ordinary skill in the art to modify Oliva et al. by including test mode operation disclosed by Whetsel in the impedance control circuit of Oliva for measuring on-resistance of output stage.

2. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oliva (US 2007/0188187 and Whetsel (US 6,731,106 B2) in view of Wong (US 7,245,144 B1).

Re claim 4, Oliva disclosed switching circuit wherein the termination resistor output stage (506) is programmable (Fig. 5).

Oliva as modified by Whetsel did not expressly disclose termination resistor input stage is programmable but would have been obvious for input stage impedance matching.

Wong (US 7,245,144 B 1) disclosed adjustable differential input and output drivers comprising adjustable termination resistances in input and output stage (drivers) to match the impedance on the differential signal lines (column 12 lines 18-27).

At the time the invention was made it would have been obvious for one of ordinary skill in the art to modify the combination system Oliva et al. and Whetsel by including programmable termination resistor in input stage for input stage impedance matching since Wong disclosed adjustable termination resistances in input stage to match the impedance on the differential signal lines.

Allowable Subject Matter

3. Claims 5-12 are allowed.

Response to Arguments

4. Applicant's arguments filed December 26, 2007 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., that the termination resistor input stage is " within a high speed data interface") are not recited in the rejected claim(s). Although the claims are interpreted in light of the

specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's arguments that "Oliva does not disclose or suggest a termination resistor input stage of a data reception signal path", the examiner asserts that Oliva does indeed disclose a termination resistor 514 input stage (chip boundary) of a data reception signal path to form an internal feedback test loop (502, 506, pad, 508 forms the feedback loop shown in Fig. 5) within said integrated circuit.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, Oliva teaches all the claimed subject matter of claims 1, 13 and 14, except that the switching transistors in the switching circuit switch in a test mode.

Whetsel discloses switching circuit for test mode operation for measuring on-resistance of an output stage (output buffer, col. 15, line 49).

The combined teaching of Oliva and whetsel would have suggested to a person of ordinary skill in the art at the time of the invention to modify Oliva by including the test mode operation disclosed by Whetsel in the impedance control circuit of Oliva for the purpose of measuring the on-resistance of the output stage.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AMY HE whose telephone number is (571)272-2230. The examiner can normally be reached on 9:30am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Diego Gutierrez/
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